Performance Characteristic of Digital Peak Current Mode Control Switching Power Supply

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Keywords

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Abstract

The purpose of this paper is to discuss performance characteristic of digital peak current mode control switching power supply. The proposed method can capture the peak current value in real time by using the voltage controlled oscillator (VCO), the programmable delay circuit and the signal frequency detector. Its transfer function is derived analytically. Also, the frequency characteristics are revealed using the loop transfer function in the case of different voltage control loop gains. In addition, its gain margin and phase margin are discussed. Furthermore, the transient responses of proposed method are compared with the conventional voltage mode control in the simulation and the experiment.

Introduction

Recently, the power consumption in IT field becomes larger because of the increase of information used. The power supply system in the data center are required to carry out the energy management for the energy saving. The digitally controlled switching power supply has attracted attention because it has many advantages such as the energy management capability, communication capability with other component, high performance control and monitoring task. These are superior features of the digital control compared with the analog control [1]-[4].

Many dc-dc converters are used as the power supply for IT equipment. Generally, the current mode control is applied to improve the stability in the analog control. Especially, the peak current mode control shows a superior transient response. However, the delay time caused by the A/D conversion time and the processing time exists in the digital control process, because the digital control circuit consists of the A/D converter and the digital controller including the digital signal processor (DSP) and the field programmable gate array (FPGA) [5]-[11]. It is the assignment of the digital control because it adversely affects the transient response. Especially, it is the critical assignment in the peak current mode control, because the peak value of current should be captured. Hence, a high-speed and expensive A-D converter is required in order to get the peak value of current correctly when the digital peak current mode control is implemented. Likewise, the digital controller which can process very

high-speed is necessary in order to turn off the main switch at the moment when the peak current is captured. Therefore, it is difficult and expensive that the peak current mode control is realized in digital control.

Accordingly, the authors have already proposed the digital peak current control circuit using the inexpensive voltage controlled oscillator (VCO) [12]. In the proposed circuit, the VCO converts the current value into the FM pulse and then it is possible to capture the peak current with the combination with the digital logic circuit and the programmable delay circuit. The transfer function and control gain of proposed method are derived in [13]. However, the design of the voltage control loop gains are not clear because the control characteristics has not discussed enough based on the analytical result.

This paper presents performance characteristics of proposed digital peak current mode control dc-dc converter. Its transfer function is derived analytically. Also, the frequency characteristics are revealed using the loop transfer function in the case of different voltage control loop gains. It has a similar shape to a primary system and improves the stability of system. Therefore, the improvement of the gain margin and the phase margin is obtained by the proposed method. Also, the transient responses are compared with the conventional voltage mode control in the simulation and the experiment. Although the transient response of the system becomes insensitive by improvement of stability, the control gain can be set to a larger value. Thus, the proposed method can improve the transient response compared with the conventional voltage mode control. In the experiment, the undershoot and the convergence time are improved by 38% and 59%, respectively. Also, the overshoot of reactor current is improved by 54%.

Operation Principle

The circuit configuration of the digital peak current mode control dc-dc converter is shown in Fig. 1. In where, E_i is the input voltage, e_O is the output voltage, R is the load, T_r is the main switch, D is the fly wheel diode, L is the energy storage reactor, i_L is the reactor current, C is the output smoothing capacitor, i_{Tr} is the switch current, R_S is the switching current detection resistor and $R_S i_{Tr}$ is the voltage equivalent to the switch current. The proposed method uses i_{Tr} instead of i_L to reduce the loss while T_r is off. The operation part of control circuit is divided into two controllers using the e_O and i_{Tr}. In the element to detect e_O, e_O is amplified to the voltage $A_{eO}e_O$, where A_{eO} is the gain of pre-amplifier of e_O. $A_{eO}e_O$ is inputted to the A/D converter and is converted into a digital value $e_O[n]$. i_{Tr} detected as $R_S i_{Tr}$ is amplified to the voltage $A_{iTr}R_S i_{Tr}$, where A_{iTr} is the gain of the pre-amplifier of $R_S i_{Tr}$, in a pre-amplifier. $A_{iTr}R_S i_{Tr}$ is inputted to the VCO. The VCO is an element which outputs the frequency modulation (FM) signal S_f depending on $A_{iTr}R_S i_{Tr}$.

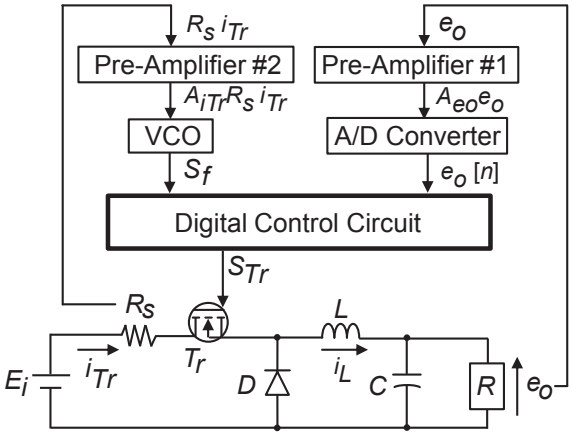


Fig. 1: Circuit configuration of the digital peak current mode control dc-dc converter.

Figure 2 illustrates the architecture of the digital control circuit. N_{PID} is the calculated value by the PID controller using $e_o[n]$ from the A/D converter. It is sent to the digital peak current detector. As shown in Fig.2, the digital peak current detector consists of the programmable delay circuit, the signal frequency detector and the digital PWM circuit. S_f from the VCO is sent to the programmable delay circuit and the signal frequency detector. Similarly, the delayed signal S_{fd} by τ from S_f is sent to the signal frequency detector. τ is the delay time determined by N_{PID}. The signal frequency detector outputs the turn off signal S_{off}. The turn on signal S_{on} generated by clock signal sets the start of the switching period. The digital PWM circuit generates the PWM signal according to S_{on} and S_{off}.

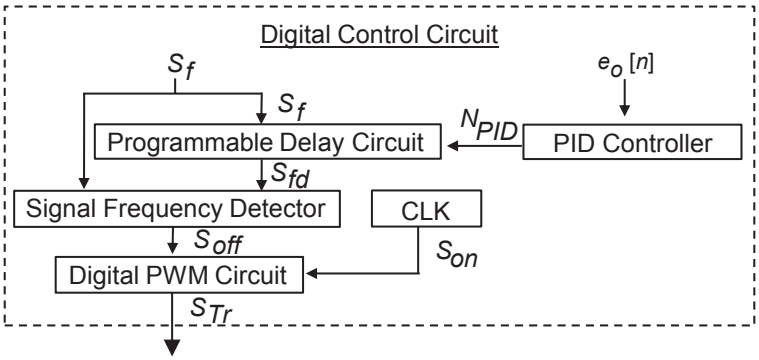


Fig. 2: Architecture of the digital control circuit.

Figure 3 shows the detail of the programmable delay circuit, the signal frequency detector and the digital PWM circuit. The multiplexer and buffers configure the programmable delay circuit. The multiplexer decides the number of buffer according to N_{PID}. Hence, S_{fd} is generated. The signal frequency detector is comprised of the RS-FF and the JK-FF and detects the frequency set by the PID control before one switching period using the phase difference between S_f and S_{fd} . In the digital PWM circuit, which consists of the RS-FF, the PWM signal S_{Tr} is generated by the turn off signal S_{off} and turn on signal S_{on}.

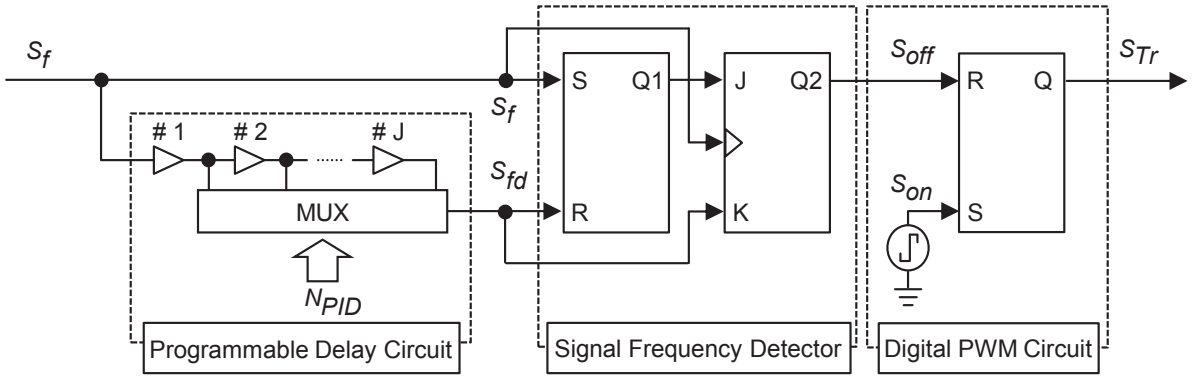


Fig. 3: Detail of the programmable delay circuit, the signal frequency detector and the digital PWM circuit.

The timing chart of the signal frequency detector is shown in Fig. 4. While PWM signal is on, the output signal Q_1 of RS-FF equals τ because rising edges of S_f and S_{fd} are inputted to the first RS-FF in

turn. In addition, the period T_f of S_f gradually becomes short because $A_{iTr}R_S i_{Tr}$ increases in linear while the PWM signal is on. The output signal of JK-FF inverts when T_f becomes shorter than τ and the clock is inputted. The digital peak current detector detects the moment as the peak value of the current and outputs S_{off}. The proposed method is able to correspond easily because the timing when S_{off} is generated is controlled by τ determined by N_{PID}.

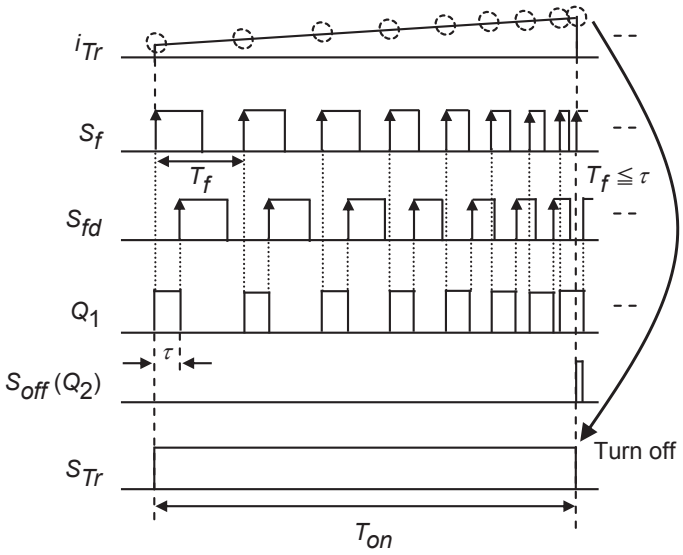


Fig. 4: Timing chart of the signal frequency detector.

Frequency Characteristics of System

Figure 5 depicts the block diagram of the digital control dc-dc converter. In where, $H(s)$ is the transfer function of the digital controller.

In the proposed method:

$$H_1(s) = H_{PIDV}(s) + \frac{H_{PC}}{R} \tag{1}$$

In the conventional voltage mode PID control:

$$H_2(s) = \frac{\left(H_P + \frac{H_I}{s} + sH_D\right)e^{-s\tau_1}}{1+s\tau_2} \tag{2}$$

In (1), $H_{PIDV}(s)$ is the transfer function of PID control in the proposed digital peak current control circuit. H_{PC} is the current gain.

$$H_{PIDV}(s) = \frac{\left(H_{PV} + \frac{H_{IV}}{s} + sH_{DV}\right)e^{-s\tau_1}}{1+s\tau_2} \tag{3}$$

$$H_{PC} = \frac{2Lf_s}{V_L} \tag{4}$$

τ_1 is the delay time of digital control and τ_2 is the time constant of anti-aliasing filter. H_{PV}, H_{IV} and H_{DV} are as follows:

$$H_{PV} = \frac{2LA_{eo}G_{AD}f_sK_{PV}}{V_L A_{iTr}R_sG_{vco}T_D{N_{PID}}^2} \tag{5}$$

$$H_{IV} = \frac{2LA_{eo}G_{AD}{f_s}^2K_{IV}}{V_L A_{iTr}R_sG_{vco}T_D{N_{PID}}^2} \tag{6}$$

$$H_{DV} = \frac{2LA_{eo}G_{AD}K_{DV}}{V_L A_{iTr}R_sG_{vco}T_D{N_{PID}}^2} \tag{7}$$

where G_{AD} is the gain of A/D converter, f_S is the switching frequency, V_L is the voltage of L, G_{VCO} is the gain of VCO, T_D is the resolution of delay buffer per one and N_{PID} is the calculation results of PID controller. K_{PV}, K_{IV} and K_{DV} are coefficients of P control, I control and D control, respectively.

In (2), H_P, H_I and H_D are as follows:

$$H_P = \frac{A_{eo} G_{AD} K_P}{N_{TS}} \tag{8}$$

$$H_I = \frac{A_{eo} G_{AD} K_I}{N_{TS} T_S} \tag{9}$$

$$H_D = \frac{A_{eo} G_{AD} T_S K_D}{N_{TS}} \tag{10}$$

where T_S is the switching period, N_{TS} is the resolution of digital PWM signal. K_P, K_I and K_D are coefficients of P control, I control and D control, respectively.

In (1) and (2), $e^{-s\tau 1}$ is approximated by

$$e^{-s\tau_1} \approx \frac{1}{1+s\tau_1} \tag{11}$$

Also, $G(s)$ is the transfer function of buck type dc-dc converter is given by

$$G(s) = \frac{\frac{1}{LC}}{s^2 + s\left(\frac{1}{CR} + \frac{r}{L}\right) + \frac{1}{LC}\left(1 + \frac{r}{R}\right)} \tag{12}$$

In (12), r is the internal loss resistance.

From Fig. 5, the loop transfer function is obtained following equation.

$$G_{Loop}(s) = E_i H(s) G(s) \tag{13}$$

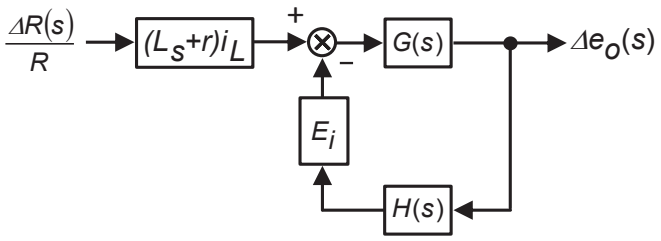


Fig. 5: Block diagram of the digital control dc-dc converter.

Figure 6 shows the bode diagram of two patterns of proposed method and conventional voltage mode PID control. In the proposed method, H_{PC} equals 2.6 A^{-1}. The blue line describes the frequency characteristics when H_{PV} is equal to 0.15 V^{-1}, H_{IV} is equal to 51 $s^{-1}\cdot V^{-1}$ and H_{DV} is equal to 0.51 $\mu s\cdot V^{-1}$. Similarly, the green line describes the frequency characteristics when H_{PV} is equal to 0.86 V^{-1}, H_{IV} is equal to 3443 $s^{-1}\cdot V^{-1}$ and H_{DV} is equal to 1.7 $\mu s\cdot V^{-1}$. In the conventional voltage mode control, the red line illustrates the frequency characteristics when H_P is equal to 0.15 V^{-1}, H_I is equal to 51 $s^{-1}\cdot V^{-1}$ and H_D is equal to 0.51 $\mu s\cdot V^{-1}$. The cut-off frequency f_C of anti-aliasing filter is 23.4 kHz. Other circuit parameters are summarized in Table I. As it is illustrated in Fig. 6, the gain characteristics of proposed method and the conventional voltage mode control have similar shape when the voltage control loop gains are the same, while their phase characteristics show different shape. Especially, the

phase of proposed method is 90 degree and leads by 180 degree compared with the conventional voltage mode control in the low frequency area. Therefore, the stability of the system is improved and the transient response shows the characteristics like a primary system. Also, the stability is not spoiled in the case of the voltage control loop gains are set to a larger value. The gain margin and the phase margin of each condition are summarized in Table II.

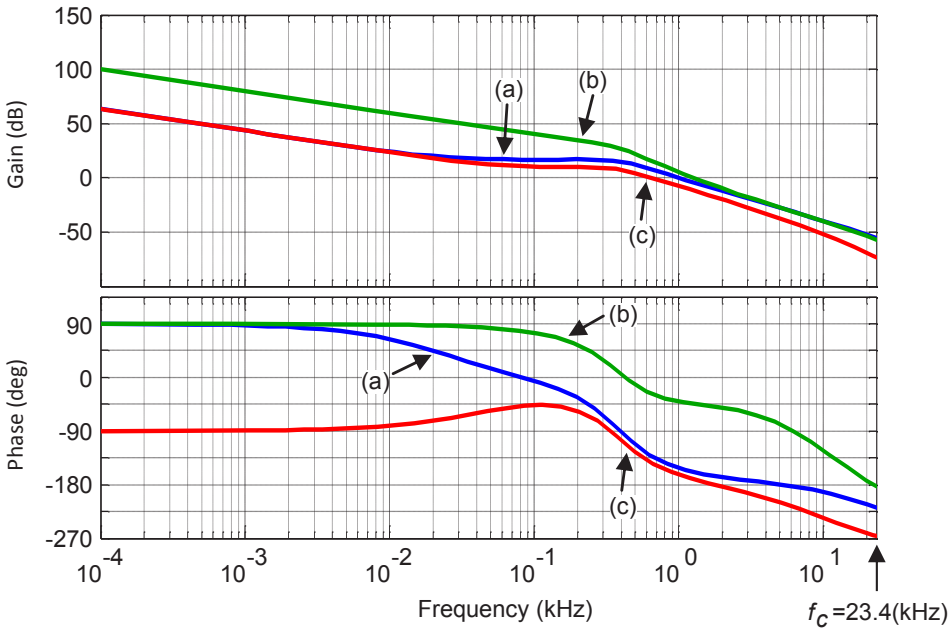


Fig. 6: Bode diagram of two patterns of the proposed method and the conventional voltage mode control: (a) the proposed method (H_{PC} = 2.6 A^{-1}, H_{PV} = 0.15 V^{-1}, H_{IV} = 51 $s^{-1}\cdot V^{-1}$ and H_{DV} = 0.51 $\mu s\cdot V^{-1}$), (b) the proposed method (H_{PC} = 2.6 A^{-1}, H_{PV} = 0.86 V^{-1}, H_{IV} = 3443 $s^{-1}\cdot V^{-1}$ and H_{DV} = 1.7 $\mu s\cdot V^{-1}$), and (c) the conventional voltage mode control (H_P = 0.15 V^{-1}, H_I = 51 $s^{-1}\cdot V^{-1}$ and H_D = 0.51 $\mu s\cdot V^{-1}$).

Table I: Circuit Parameters in Loop Transfer Function

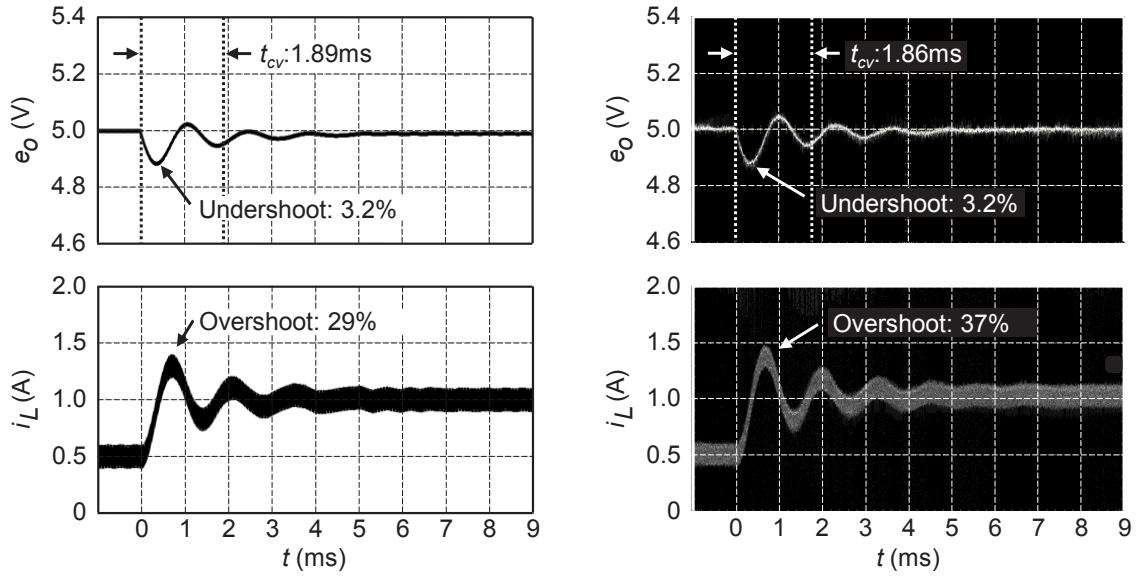
E_i	20 V	R_S	0.05 Ω
E_o*	5 V	A_{iTr}	39
r	0.5 Ω	A_{eo}	0.25
L	194 μH	G_{AD}	409.4 V^{-1}
V_L	20 V	G_{VCO}	3.02 MHz·V^{-1}
C	990 μF	T_D	1 ns
R	5 Ω	N_{Ts}	2000
f_S	100 kHz	N_{PID}	511
T_S	10 μs		

Table II: Gain Margin and Phase Margin in Each Condition

	Gain Margin	Phase Margin
(a)	28.5 dB	28.1 degree
(b)	135 dB	55.8 degree
(c)	36.2 dB	17.9 degree

Transient Response

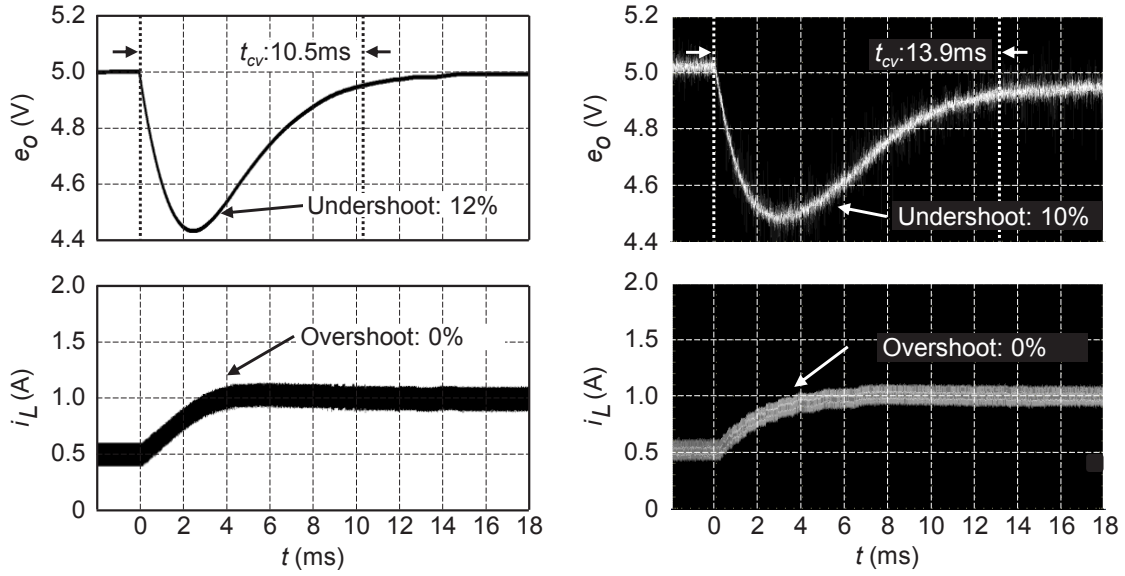
The transient responses of proposed method and conventional voltage method are shown in Figs. 7 through 9. The step change R_{step} of the load is 10 Ω to 5 Ω. The simulator is PSIM. When the main switch is on, the internal loss resistance r_1 of dc-dc converter is 0.5 Ω. When the main switch is off, the internal loss resistance r_2 of dc-dc converter is 0.2 Ω. Other circuit parameters are indicated in Table III. Evaluated items are the undershoot of e_o, the overshoot of i_L and the convergence time t_{cv} when the output voltage converges within 1% from the reference voltage. In the conventional voltage mode control, the control gain has already mentioned above. As Fig. 7 shows, the under shoot is 3.2 %, t_{cv} is 1.89 ms and the overshoot of i_L is 29% in the simulation. Also, the under shoot is 3.2%, t_{cv} is 1.86 ms and the overshoot of i_L is 37% in the experiment. The transient responses of the proposed method whose gain is the same as the blue line in Fig. 6 are shown in Fig. 8. The undershoot is 12%, t_{cv} is 10.5 ms and the overshoot of i_L is 0% in the simulation. In the experiment, the under shoot is 10%, t_{cv} is 13.9 ms and the overshoot of i_L is 0% in the experiment. The transient response becomes slow because the stability of the system is improved by applying the proposed method. Therefore, the control gain can be set to a larger value compared with the conventional voltage mode control. The



(a) Simulation. (b) Experiment.

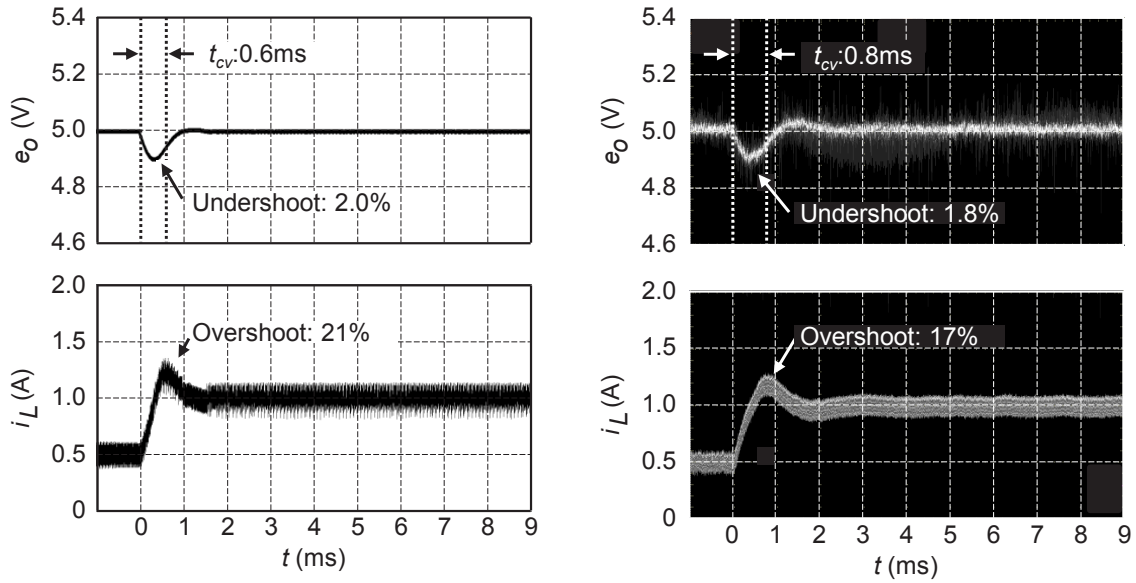
Fig. 7: Transient response of the conventional voltage mode PID control in the simulation and the experiment (H_P = 0.15 V^{-1}, H_I = 51 $s^{-1}\cdot V^{-1}$ and H_D = 0.51 $\mu s\cdot V^{-1}$).

transient responses of the proposed method whose gain is the same as the green line in Fig. 6 are shown in Fig. 9. It indicates a superior transient response to conventional voltage mode PID control. The undershoot is 2.0%, t_{CV} is 0.62 ms and the overshoot of i_L is 21% in the simulation. In the experiment, the under shoot is 1.8%, t_{CV} is 0.80 ms and the overshoot of i_L is found as 17% in the experiment. The large control gain brings the improvement of transient response of proposed method. However, the



(a) Simulation. (b) Experiment.

Fig. 8: Transient response of the proposed method in the simulation and the experiment (H_{PC} = 2.6 A^{-1}, H_{PV} = 0.15 V^{-1}, H_{IV} = 51 $s^{-1}\cdot V^{-1}$ and H_{DV} = 0.51 $\mu s\cdot V^{-1}$).



(a) Simulation. (b) Experiment.

Fig. 8: Transient response of the proposed method in the simulation and the experiment (H_{PC} = 2.6 A^{-1}, H_{PV} = 0.86 V^{-1}, H_{IV} = 3443 $s^{-1}\cdot V^{-1}$ and H_{DV} = 1.7 $\mu s\cdot V^{-1}$).

Table III: Circuit Parameters in Simulation

E_i	20 V	f_S	100 kHz
$E_o{}^*$	5 V	T_S	10 μs
$r1$	0.5 Ω	A_{iTr}	39
$r2$	0.2 Ω	A_{eo}	0.25
V_D	0.3 V	G_{AD}	409.4 V^{-1}
L	194 μH	G_{VCO}	3.02 MHz·V^{-1}
V_L	20 V	T_D	1 ns
C	990 μF	N_{Ts}	2000
R_{step}	10 Ω→5 Ω		

system becomes unstable and oscillates when the control gain of conventional voltage mode PID control is set to the same value with Fig. 9.

Conclusion

This paper presents a performance characteristic of digital peak current mode control switching power supply. The frequency characteristics of the proposed method are revealed and compared with the conventional voltage mode control. According to the bode diagram, the phase of proposed method is 90 degree and leads by 180 degree compared with the conventional voltage mode control in the low frequency area. Therefore, the improvement of stability is obtained and the transient response shows the characteristics like a primary system. Although the transient response of the system becomes slow by getting stable, the control gain can be set to a larger value. In the case of the large gain of voltage control loop, the stability is kept up as shown in the bode diagram. Thus, the proposed method can improve the transient response compared with the conventional voltage mode control. It is confirmed in the simulation and experiment. In the experiment, the undershoot, the convergence time and the overshoot of reactor current are improved by 38%, 59% and 54%, respectively.

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