A Consideration of Signal Frequency Detector in Digital Peak Current Mode DC-DC Converter

Yudai Furukawa*, Shusuke Maeda*, Shunsuke Tsuruoka*, Fujio Kurokawa*, Haruhi Eto† and Ilhami Colak‡
*Graduate School of Engineering, Nagasaki University, Nagasaki, Japan
e-mail: bb52215203@cc.nagasaki-u.ac.jp
†Faculty of Engineering, Nagasaki Institute of Applied Science, Nagasaki, Japan
e-mail: haruhi-eto@awa.bbiq.jp
‡Faculty of Engineering and Architecture, Gelisim University, Istanbul, Turkey
e-mail: icolak@gelisim.edu.tr

Abstract— **The purpose of this paper is to reveal the designing of the static characteristic of the digital peak current mode dc-dc converter using a voltage controlled oscillator (VCO). In the proposed method, it is able to sample the reactor current by using the VCO and the delay circuit. The improvement of the dynamic characteristic and the analysis of the proposed method have already been revealed. However the design method in the static characteristic of the proposed method has not been clear. In this paper, the analysis about the resolution of the output voltage is revealed for the designing of the proposed method in static characteristic. The change of the output voltage against the change of the delay time in the signal frequency detector is confirmed by comparing the analysis result and simulation results. Furthermore, the effect, which the signal frequency detector gives to the output voltage in the transient state, is discussed.**

Keywords- dc-dc converter; digital control; peak current mode

I. INTRODUCTION

Recently, the introduction of the renewable energy is necessary because the fossil fuel depletion is concerned. However, the renewable energy has the disadvantage that the stable supply of electric power is difficult because of the dependence on the environmental conditions. The reduction of the power consumption in the electronic device is important in order to efficiently utilize such energy. Therefore, the efficient operation with the monitoring function of the power consumption by the digital control technology attracts attention in order to energy saving. [1], [2].

The current mode is used to stabilize the system [3], [4]. In the conventional analog control, it has been implemented. It is also considered to implement a peak current mode by digital control [5]. However the high speed A-D converter is necessary to detect the peak value of the current. In addition, the high speed digital signal processor (DSP) is required. That is why it is difficult to implement or tends to become expensive. The proposed method does not need the high speed A-D converter because it uses the voltage controlled oscillator (VCO) for the sampling of the current. Therefore, it is possible to detect the peak value of the current in real time. The transient response of the proposed method has already discussed. On the other hand, the static characteristics has not been revealed. It is necessary for the design of the proposed method.

This paper presents the relationship between the delay time of the delay circuit and the output voltage by the analysis based on the equation of the on time of the switch and the output voltage. The influence that the frequency detection circuit of the proposed method affects the output voltage in static characteristics is discussed.

II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

Figure 1 shows the circuit diagram of the digital peak current mode dc-dc converter. E_i is the input voltage, e_o is the output voltage, L is the inductor, C is the capacitor, D is the diode, R is the load resistance, T_r is the switch, i_{Tr} is the switch current and R_s is the sense resistor of the switch current. The control circuit is consisted of the output voltage detector and the switch current detector.

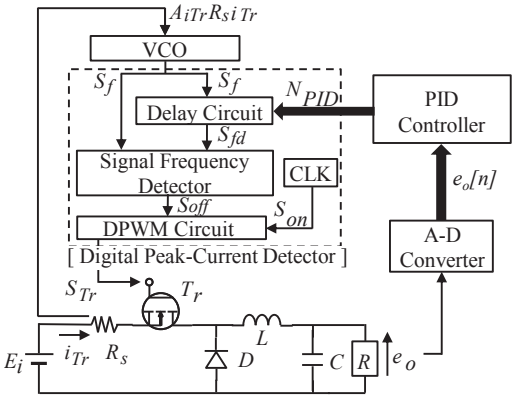

Figure 1. Circuit diagram of digital peak current mode dc-dc converter.

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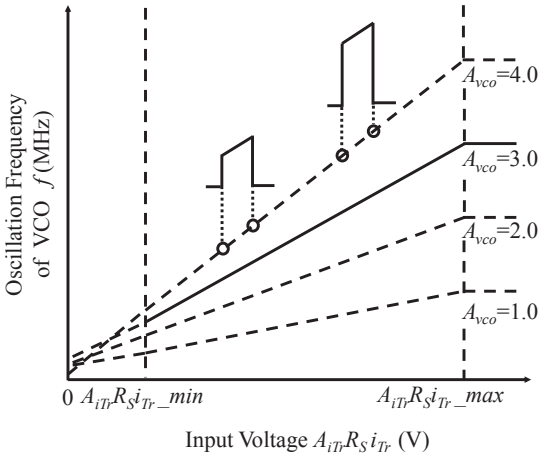

Figure 2. Input-output characteristics of VCO.

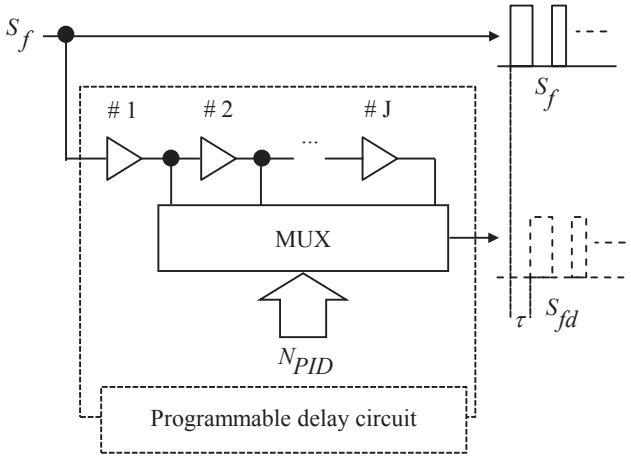

Figure 3. Configuration of programmable delay circuit.

In the output voltage detector, the PID control calculation is performed based on the detected e_O, the calculation value N_{PID} is sent to the digital peak current detector. N_{PID} is represented by the following (1).

$$N_{PID} = N_B - K_P\left(e_o[n-1] - N_R\right) - K_I - \sum_{k=1}^{n}\left(e_o[n-1] - N_{INT}\right) - K_D\left(e_o[n] - e_o[n-1]\right) \quad (1)$$

where N_B is the control bias value, K_P is the proportional coefficient, K_I is integral coefficient, K_D is the differential coefficient, N_R is the reference value of the proportional control, N_{INT} is the reference value of the integral control, $e_O[n]$ and $e_O[n\text{-}1]$ is the digital value of e_O in the n-th and the (n-1)-th switching period.

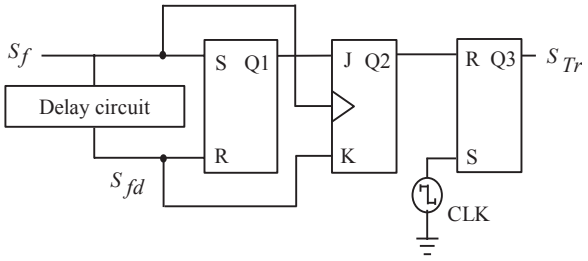

Figure 4. Circuit diagram of signal frequency detector and DPWM signal generator.

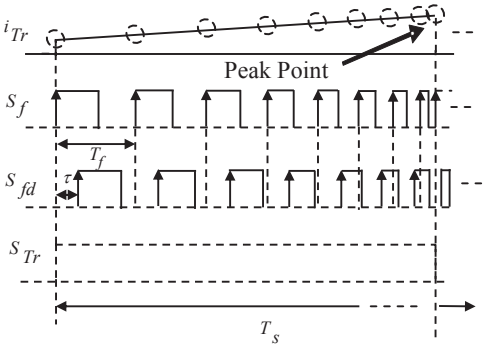

Figure 5. Timing chart of proposed digital peak current detector.

In the switch current detector, i_{Tr} is sent to the VCO through R_S as the voltage value $A_{iTr}R_S i_{Tr}$. A_{iTr} is the gain of the preamplifier in the current detector.

The input-output characteristic of the VCO is shown in Fig. 2. The VCO is the element that outputs the FM pulse signal S_f. Its oscillation frequency f is proportional to the input voltage value. f is expressed by the following equation.

$$f = A_{VCO}\left(A_{iTr}R_s i_{Tr} + E_B\right) + B \quad (2)$$

where A_{VCO} is the gain of the VCO and E_B is the voltage value of the DC bias in the preamplifier for the switch current. B is the intercept when the input-output characteristic of the VCO is approximated linearly. Furthermore, the period T_f of S_f is expressed by (3).

$$T_f = \frac{1}{f} = \frac{1}{A_{VCO}\left(A_{iTr}R_s i_{Tr} + E_B\right) + B} \quad (3)$$

T_f becomes gradually shorter because the i_{Tr} increases linearly when the switch of the main circuit is on.

The digital peak current detector is consisted of the programmable delay circuit, the signal frequency detector. S_f is sent to the signal frequency detector and the programmable delay circuit. The configuration of the programmable delay circuit is shown in Fig. 3. T_D is the

resolution of the delay buffer per one. S_f sent to the programmable delay circuit passes delay buffers in accordance with N_{PID}. This signal is a signal S_{fd} obtained by delaying by the delay time τ. τ is expressed by the following equation.

$$\tau = T_D N_{PID} \tag{4}$$

S_{fd} is also sent to the signal frequency detector.

Figure 4 shows the circuit diagram of the signal frequency detector and DPWM signal generator. The signal frequency detector is consisted of RS-FF, JK-FF and the programmable delay circuit. It detects the signal frequency by using a phase difference between S_f and S_{fd}. Its output signal and the clock signal are sent to the DPWM signal generator. The DPWM signal generator outputs the PWM signal S_{Tr} depending on them.

Figure 5 shows a timing chart of the digital peak current detector during one switching period T_S. i_{Tr} increases linearly while T_r is on. Thus, T_f shortens gradually. The proposed peak current detector is able to detect the peak point of i_{Tr} in real time. At the moment when T_f becomes shorter than τ, the peak current is detected. Simultaneously, the digital peak current detector turns off T_r. The peak value of i_{Tr} is selected optimally by the PID control.

III. Analysis of Stasic Characteristics

The signal frequency detector in the proposed method affects the resolution of the output voltage. So, its resolution is discussed. In [6], the on time T_{on} of T_r is derived as follows.

$$T_{on} = \frac{2L}{E_i - E_o}\left\lfloor \frac{1}{A_{iTr}R_s}\left\{\frac{1}{A_{VCO}}\left(\frac{1}{\tau} - B\right) - E_B\right\} - I_L \right\rfloor \tag{5}$$

The equation of the relationship between the input and the output voltage of the buck converter considering the loss of the circuit as the internal resistance r is (6).

$$E_o = \frac{\frac{T_{on}}{T_s}}{1 + \frac{r}{R}} E_i \tag{6}$$

In (6), the equation of the output voltage E_O is expressed by a substitution (5) for T_{on}.

$$E_o = \frac{2Lf_s E_i\left\lfloor \frac{1}{A_{iTr}R_s}\left\{\frac{1}{A_{VCO}}\left(\frac{1}{\tau} - B\right) - E_B\right\} - I_L \right\rfloor}{\left(E_i - E_o\right)\left(1 + \frac{r}{R}\right)} \tag{7}$$

The resolution of the output voltage against τ is expressed by (8) considering the small change Δe_O and $\Delta\tau$ of e_O and τ.

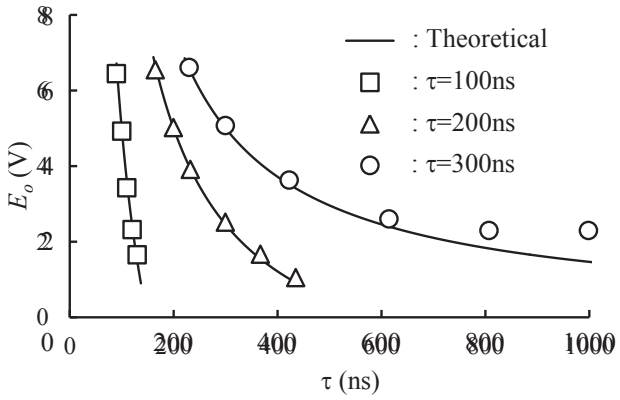

Figure 6. Relationship between τ and E_O.

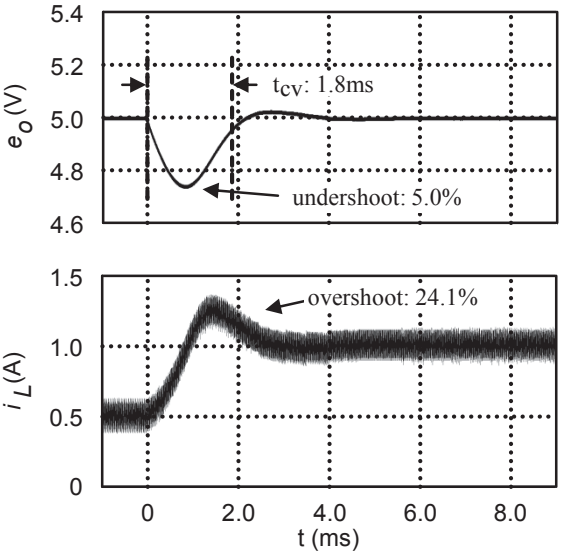

Figure 7. Transient response (τ=300ns).

$$\frac{\Delta e_o}{\Delta\tau} = \frac{2Lf_s E_i}{A_{iTr}R_s A_{VCO}\tau^2\left(1 + \frac{r}{R}\right)\left\{E_i - 2E_o + \frac{2Lf_s E_i}{R + r}\right\}} \tag{8}$$

Figure 6 shows the relationship between τ and E_O. It is compared the simulation value and the theoretical value based on the analysis result. The rated output voltage and the output current of the proposed scheme are 5 V and 1 A. The white square, the white triangle and the white circle denote the simulation value in each case, which the delay time τ is 100 ns, 200 ns and 300 ns at the rated. The lines show the theoretical value in those cases. The switch current is operated from 0.2 A to 1.5 A in the proposed method. Therefore, the operating range of the oscillation frequency also changes as shown in Fig.6 by changing the value of the oscillation frequency at the rated. Theoretical values are calculated regarding the rated as the standard. Therefore, the error nearby rated is small and in the away range from the

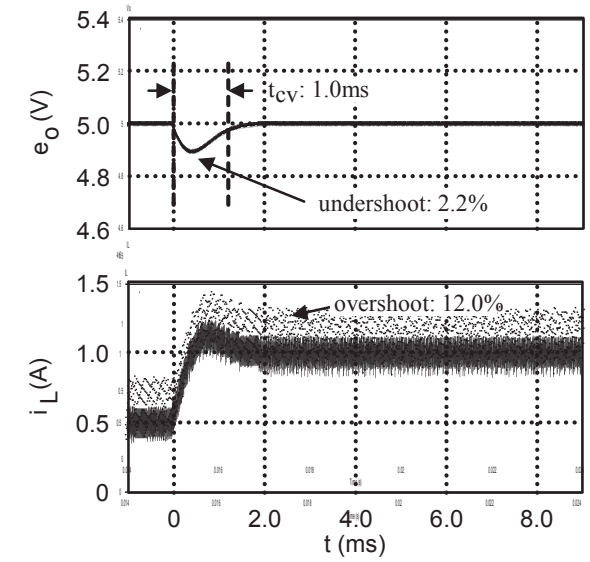

Figure 8. Transient response (τ=200ns).

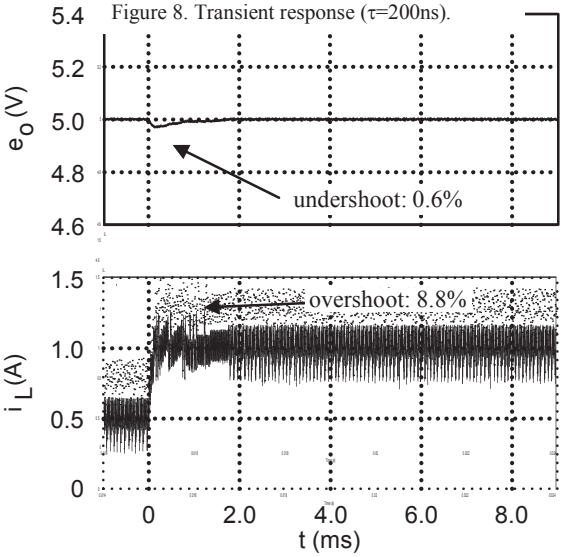

Figure 9. Transient response (τ=100ns).

rated becomes larger. The simulation value and the theoretical one are well accorded in the area, where τ is small. The error between the theoretical and simulation value becomes larger when τ is large. The changes of the output voltage in each case are about 17mV, 39mV and 155mV when τ is around the rated. Moreover, they become small when the τ is large.

Figures 7 through 9 show the transient response when the load changes stepwise from 10 Ω to 5 Ω in the cases that τ are 300 ns, 200 ns and 100 ns. The t_{cv} is the convergence time to settle into ± 1% of the reference value of the output voltage. Each of the control coefficient is K_P = 5, K_I = 0.1 and K_D = 1. In Fig. 7, the overshoot is 24%, the undershoot is 5% and t_{cv} is 1.8 ms. Also, the overshoot is 12%, the undershoot is 2.2% and t_{cv} is 1.0 ms in Fig. 8. Figure 9 indicates the overshoot, the undershoot which are 8.8% and

TABLE I. CIRCUIT PARAMETERS

E_i	20 (V)
E_o	5 (V)
R	5 (Ω)
r	0.5 (Ω)
L	194 (μH)
C	990 (μF)
f_S	100 (kHz)
R_S	0.05 (Ω)
A_{iTr}	39
A_{VCO}	3.02 (MHz/V)
B	-3.36 (MHz)
E_B	1.4 (V)
T_D	1 (ns)

0.6%, respectively. The transient response becomes quick when τ is small, namely, N_{PID} is small because the control gains vary according to (9) through (11). These are derived in [7].

TABLE II. CIRCUIT PARAMETERS

$$H_{PV} = \frac{2LK_P A_{eo} G_{AD} f_s}{V_L A_{iTr} R_s A_{VCO} T_D N_{PID}^2} \quad (9)$$

$$H_{IV} = \frac{2LK_I A_{eo} G_{AD} f_s^2}{V_L A_{iTr} R_s A_{VCO} T_D N_{PID}^2} \quad (10)$$

$$H_{DV} = \frac{2LK_D A_{eo} G_{AD}}{V_L A_{iTr} R_s A_{VCO} T_D N_{PID}^2} \quad (11)$$

On the other hand, the resolution of the output voltage becomes coarse as described above.

IV. CONCLUSION

In this paper, the relationship between the output voltage and the delay time of the programmable delay circuit in the signal frequency detector is derived. Moreover, the resolution of the output voltage in the proposed method is revealed from the obtained relationship. The validity of

them is confirmed by the comparison of the theoretical value with the simulation value. When the delay time becomes a larger value, the resolution of the output voltage becomes fine. It is possible to obtain a fine resolution by considering the relationship between the operating range of the VCO and the delay time. Meanwhile, the transient response is better when the delay time becomes a smaller value. Hence, these relationships are considered to design.

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