Seven Level Asymmetric Cascade Inverter with Space Vector PWM Added PR Control

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***Abstract*-Inverters are used to convert the DC energy to AC energy for renewable energy conversation or high power industrial applications. Asymmetric inverters are preferred about their some advantages. Nowadays, control of inverters is achieved lots of pals with modulation (PWM) techniques. Space vector control is one of them. Seven level asymmetric cascade inverter is achieved with space vector PWM (SVPWM) added proportional resonant (PR) control in this study. The PR control is used for reducing the lower number harmonics. General SVPWM techniques use position of a vector in αβ frame. Calculation of switching states becomes more complex when the level of inverter is increased. In this study, switching states is achieved with ceil and floor operations by using reference signals in 60^0 degree coordinate system. Switching signal is generated depends on output levels of inverter. This process is mitigated calculations in SVPWM. Also adding PR control to system decreases the total harmonic distortion (THD) of inverter.**

I. INTRODUCTION

In recent years, multilevel inverters (MLIs) are being used more often in medium voltage and high power industrial applications. MLIs have some advantages about common mode voltage, dv/dt ratio and THD. There are three different topologies of MLIs such as the diode-clamped, the flying capacitor and the cascaded H-bridge. The cascaded MLIs are classified into two categories that are symmetric and asymmetric topologies depending on dc-link voltage ratio of cells. The sources of symmetric MLIs are supplied at the equal amplitudes while that of asymmetric cascade MLIs (ACMLIs) are at different amplitudes as shown in Fig. 1. Two types of ACMLIs are configured either in binary where the ratio of cells is increasing the power of two as V, 2V, 4V or in trinary that ratio of cells is increasing the power of three as V, 3V, 9V. ACMLIs are needed less number of switching components when compared other types of MLIs. [1-5]

There are many switching techniques improved for MLIs such as SVPWM, multicarrier PWM, selective harmonic elimination and hybrid PWM. [1, 5-7]. The most popular technique is SVPWM for three phase MLIs [8]. SVPWM technique can be implemented with digital signal processing, and also implementation and optimization of switching pattern is easy [9, 10].

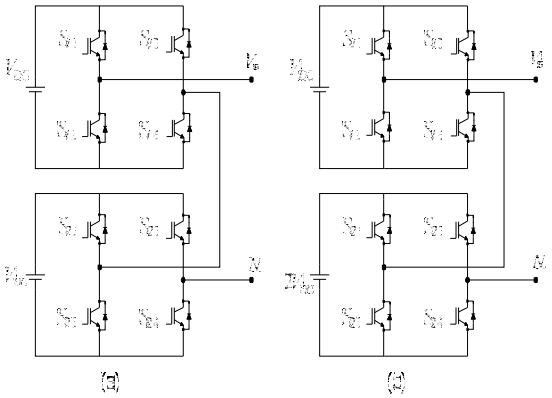

Fig. 1. Cascade MLIs categories (a) symmetric MLIs, (b) asymmetric MLIs

Voltage control and current control are two different ways of controlling the inverters. Common current control techniques are proportional integral, PR control, repetitive controller, predictive control, dead beat and hysteresis control as depicted in Fig. 2. [11-14]

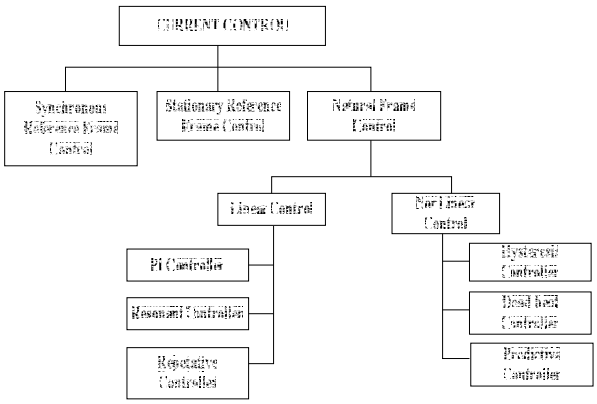

Fig. 2. Current control methods

Seven-Level ACMLI (binary type) simulation is performed with SVPWM, adding PR control techniques in this paper. SVPWM and PR control is explained in Section II while the simulation structures and results are given in Section III. Discussion of results is mentioned in Section IV.

II. SVPWM AND PR CONTROL

A. SVPWM

SVPWM technique is started to be used in the middle of 1980's. It is digital modulation technique that generates switching states with sampling a reference vector. Reference vector is moving in αβ frame (90^0 coordinate system). This coordinate system is divided into six parts, which are called as sectors with 60^0 angle difference (15, 16).Input signals are converted to αβ frame with Clarke transfer functions. Traditional SVPWM uses αβ frame, but Wei et al. [17] developed a new coordinate system using 60^0 degree coordinate system. Equation (1), (2) and (3) show transfer functions of Clarke transfer functions and V_a, V_b, V_c are input signals, V_α and V_β are signals in αβ frame, V_{ref} is amplitude of reference signal and θ is angle of reference signal, respectively.

$$\begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} = \frac{2}{3} \times \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \times \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \quad (1)$$

$$|Vref| = \sqrt{V\alpha^2 + V\beta^2} \quad (2)$$

$$\theta = \tan^{-1} \frac{V_\beta}{V_\alpha} \quad (3)$$

Equation (4), (5) and (6) are used to transfer the reference signals from αβ frame to 60^0 degree coordinate system. In these equations, V is the normalization parameter of transfer function, m is the modulation index, V_{dc} is total of input DC sources and h is the level of inverter. V_x and V_y are the signals in 60^0 degree coordinate system. Fig. 3 shows V_x and V_y in 60^0 degree coordinate system for first sector. Simulation diagram and V_x and V_y signals are proposed in Fig. 4 and Fig 5, respectively.

$$V = \frac{Vref \cdot m \cdot (h-1)}{Vdc} \quad (4)$$

$$V_x = |(V \times \cos\theta) - (V \times \sin\theta / 3)| \quad (5)$$

$$V_y = |(V \times \cos(60-\theta)) - (V \times \sin(60-\theta) / \sqrt{3})| \quad (6)$$

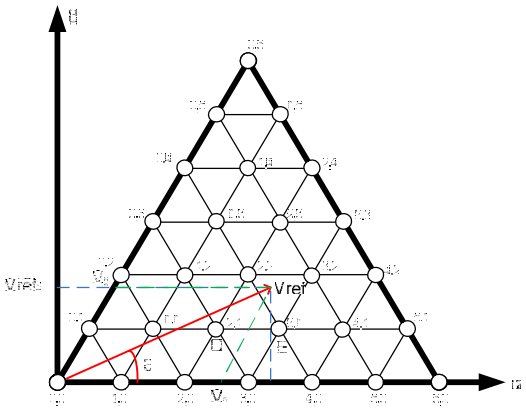

Fig. 3. V_x and V_y in 60^0 degree coordinate system

In traditional SVPWM techniques the switching states is, produced in the following way for one phase. Positive peak value is during two sectors, negative peak value is during two sectors and passing from positive peak to negative peak and passing from negative peak to positive peak is during two sectors.

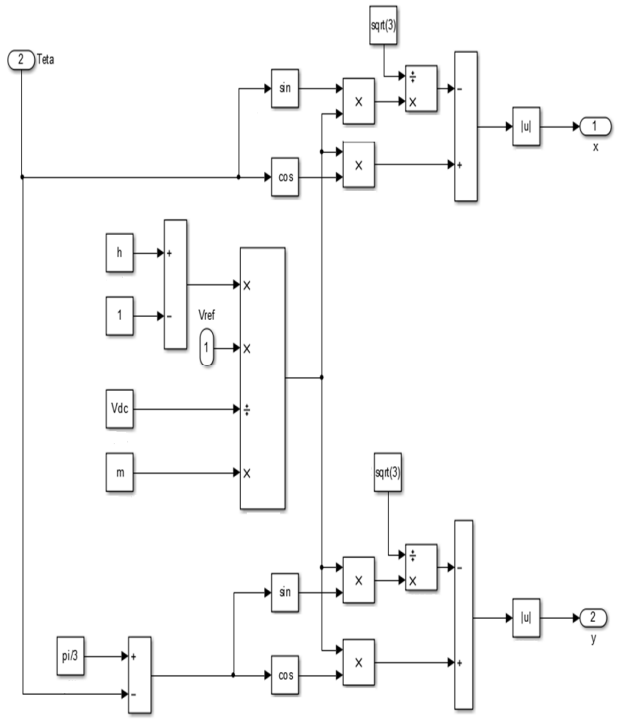

Fig. 4. Simulation diagram of degree coordinate system transfer block

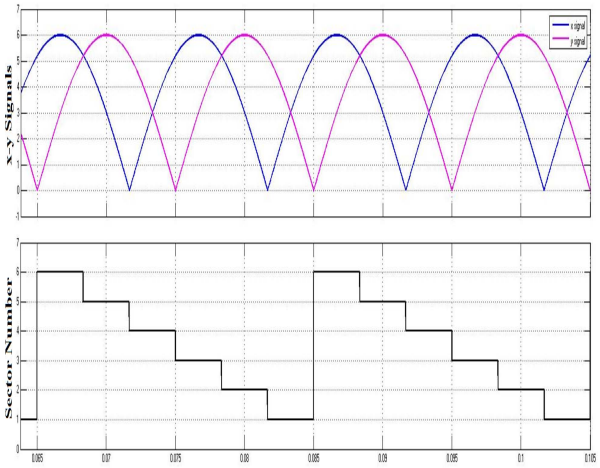

Fig. 5. V_x and V_y signals and Sector numbers

Celanovic and Boroyevich [18] and Prats et al. [19] performed SVPWM with ceil and floor operators. In this paper, SVPWM performed with this suggestion and additional to these switching states are generated with using 60^0 degree reference signals to calculating of inverters outputs instead of calculating vector positions of reference signals. Calculations of SVPWM are reduced by this way.

First of all, the output of inverter in each sector should be known for the switching states of the calculation process. Table 1 indicates the output of inverter sector by sector for one phase. As shown in Table I, signals of phases trace a sequence. The sequence is positive peak value at one sector, passing from positive peak to negative peak at two sectors, negative peak value at one sector and passing from negative peak to positive peak at two sectors. For a seven level of ACMLI the outputs are 3V, 2V, V, 0, -V, -2V and -3V while input DC sources are V and 2V.

TABLE I
OUTPUTS OF INVERTER FOR EACH SECTOR

	Phase A	Phase B	Phase C
Sector 1	3V	-V, -2V	-V, -2V
Sector 2	V, 2V	V, 2V	-3V
Sector 3	-V, -2V	3V	-V, -2V
Sector 4	-3V	V,2V	V, 2V
Sector 5	-V, -2V	-V, -2V	3V
Sector 6	V, 2V	-3V	V, 2V

The switching signals are generated with digital techniques in SVPWM for driving the semi-conductors. Belong to this, we can operate normalized reference signals with ceil and floor operators. Equation (7), (8), (9) and (10) shows ceil and floor values of V_x and V_y signals. These are *xc, xf, yc, yf*, respectively.

Ceil operation rounds the number towards positive infinity and floor operation rounds the number towards negative infinity. Sector number and *xc*, *yc*, *xf* and *yf* signals are shown in Fig. 6. The value of *xc* and *yc* are integer numbers between 1 and 6. The value of *xf* and *yf* are integer numbers between 0 and 5. Calculations are indicated in Table II to realize switching states of inverter for each phase. Switching states of one phase is shown in Fig 7. There are eight output of SVPWM for one phase.

$$xc = ceil(x) \tag{7}$$

$$xf = floor(x) \tag{8}$$

$$yc = ceil(y) \tag{9}$$

$$yf = floor(y) \tag{10}$$

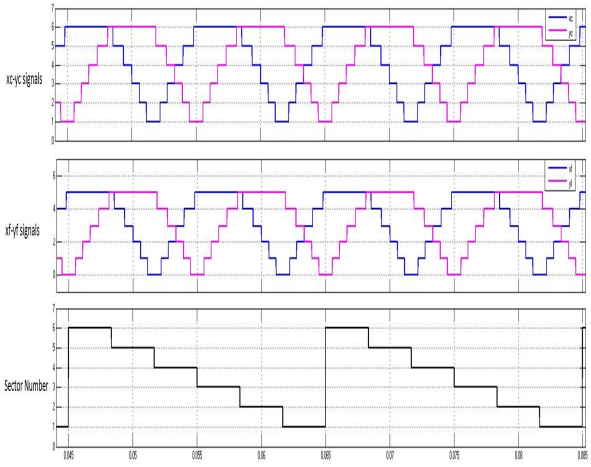

Fig. 6. xc, yc, xf and yf signals at sectors

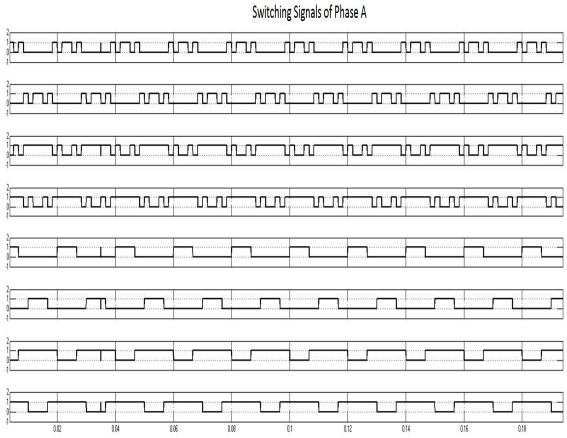

Fig. 7. Switching states of one phase

TABLE II
CALCULATION OF SWITCHING STATES

	Phase A	Phase B	Phase C
Sector 1	Floor((xc+yc)/2)	-Ceil(xc/3)	-Ceil(yc/3)
Sector 2	-Floor((xf-yc)/3)	Ceil(xc/3)	-Ceil(yc/2)
Sector 3	-Ceil((xc-yc)/3)	Ceil(xc/2)	-Ceil(yc/3)
Sector 4	-Floor((xc+yc)/2)	Ceil(xc/3)	Ceil(yc/3)
Sector 5	Floor((xf-yc)/3)	-Ceil(xc/3)	Ceil(yc/2)
Sector 6	Ceil((xc-yc)/3)	-Ceil(xc/2)	Ceil(yc/3)

B. PR Control

The PR control in this study is achieved in natural frame. The PR control transfer function is defined in (11) where ω is the resonance frequency, K_p is the proportional gain, K_i is the integral gain of the PR controller and s is the integration term in s domain. [20-22]

$$G_{PR}(s) = K_p + K_i \frac{s}{s^2 + w^2} \tag{11}$$

Main operating principle of PR control is that the system can adjusts gain only desired at a specific frequency. Low order harmonics can be eliminated with PR control. It is capable to track the sinusoidal reference with zero steady-state error. General structure of PR control is shown in Fig. 8 where the output current of the inverter is compared with a reference signal and transfer function is implemented for each phases. [20-22]

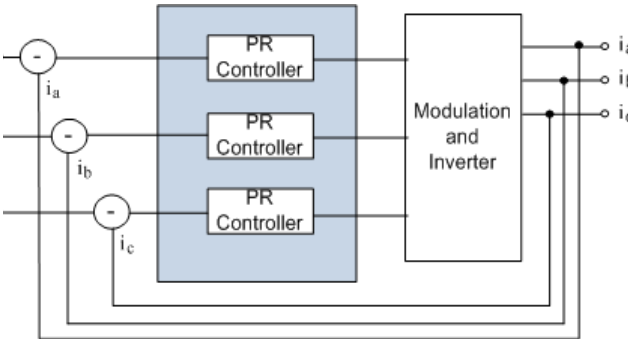

Fig. 8. General structure of PR control

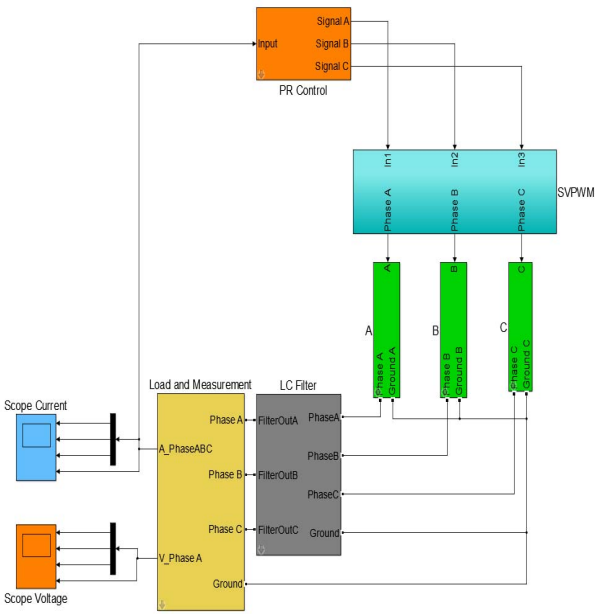

Fig. 9. Simulation diagram of Seven Level ACMLI

III. SIMULATION OF SEVEN LEVEL ACMLI

Main simulation diagram is shown in Fig. 9. There are different blocks such as H-Bridges, SVPWM, PR Control, filter and Load. H-Bridges is connected like Fig. 1(b). *LC* filter parameters are 5mH and 500µF, respectively. Load is star connected *RL*, 5Ω and 20 mH, respectively.

SVPWM block generates switching signals and there are different sub-blocks as depicted in Fig. 10. Sub-blocks of SVPWM convert three phase signals which connected to PR control outputs to αβ frame and gets V_{ref} and θ parameters. Then coordinate sub-block converts the αβ frame to 60^0 degree coordinate system. Switching states sub-block performs calculations of switching states according to sector numbers.

PR control block compares the output of ACMLI with reference signal as shown in Fig. 11. Output current of inverter is compared with reference signals. PR control gain is implemented to phases separately. K_p parameter is 1 and K_i parameter is 1.1 in PR control in this study. Output of PR control block is connected to SVPWM block for input signals for generation switching states.

Filtered three phase line voltages are illustrated in Fig. 12. Output voltage levels are equal to each other as a value of 300V. Input voltage values of sources are 100V and 200V in H-Bridges. Also filtered three phase line currents are shown in Fig. 13, as can be seen here phase differences of the output currents of inverter are 120^0.

THD of output voltage (THDv) is 2.16%and THD of output current (THDc) is 0.79%as given in Fig. 14 and Fig. 15, respectively. Harmonic orders are taken to the fiftieth harmonic. Harmonic orders from 13-50 are nearly at zero level and lower harmonics of THDv and THDc are mitigated.

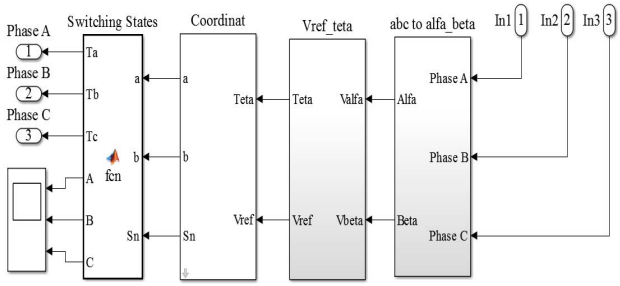

Fig. 10. SVPWM block

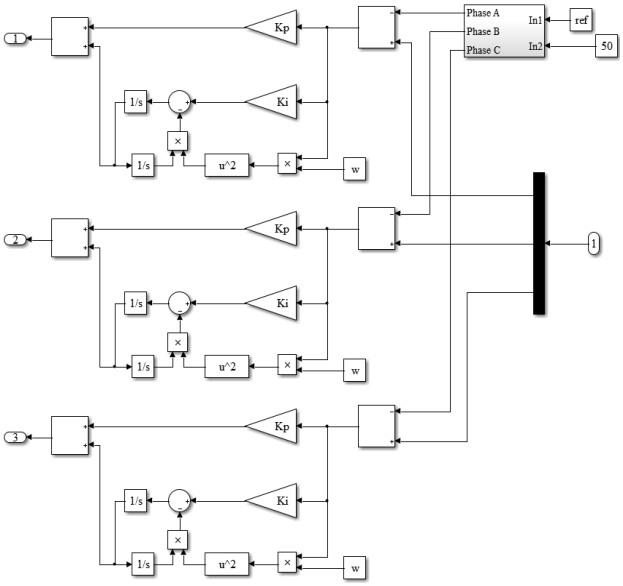

Fig. 11. PR control block

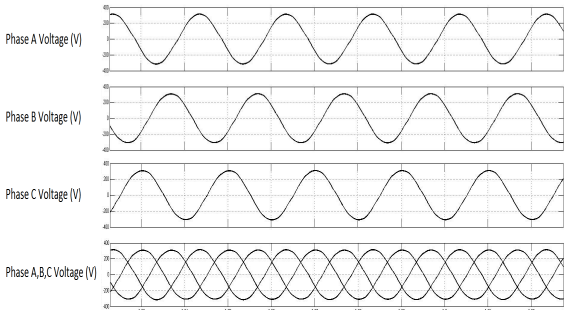

Fig. 12. Output voltages of inverter

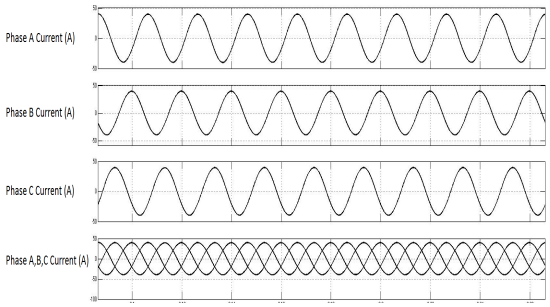

Fig. 13. Output currents of inverter

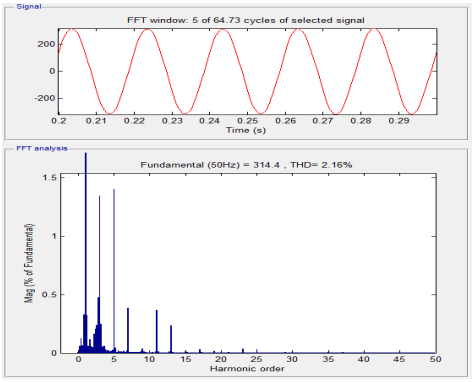

Fig. 14. THD of output voltage

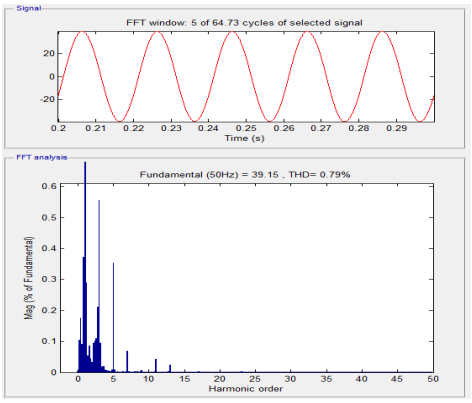

Fig. 15. THD of output current

IV. CONCLUSIONS

This study proposes a SVPWM controlled ACMLIs with adding PR control. General SVPWM controllers use vector calculation for switching states. This study uses ceil and floor operations for calculation of switching states by using output levels of inverter. This method is used, hence, for the complex calculations and look-up tables are not needed. There are a lot of unused vectors in general SVPWM systems. This technique can be implemented for the high level ACMLIs by only calculation the output level of inverter. In further studies, the adaptive control algorithms can be implemented to PR control for different parameter of loads.

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